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ERROR CONTROL CODING METHOD AND SYSTEM FOR NON-VOLATILE MEMORY

TECHNICAL FIELD

001 The present invention relates to non-volatile memory devices. The present invention also relates to methods and systems for improving the repairing efficiency of non-volatile memory devices. The present invention additionally relates to Error Correction Coding (ECC) methods and systems.

BACKGROUND OF THE INVENTION

002 Non-volatile memory design based on integrated circuit technology represents an expanding field. Non-volatile memory devices are generally configured as storage systems or devices that do not lose data when power is removed from the storage system or device. Several types of non-volatile memory devices are currently utilized in computers and other data-processing devices. The most commonly utilized non-volatile memory devices fall into three primary categories: EPROM, EEPROM and Flash memory.

003 The first type of commonly utilized non-volatile memory is Erasable Programmable Read-Only Memory (EPROM). EPROM is a type of non-volatile memory that can be reprogrammed after it is manufactured. EPROMS can generally be reprogrammed by removing the protective cover from the top of the EPROM computer chip and exposing the chip to ultraviolet light. EPROM is more

than 20 years old and is popular for program storage because EPROM is inexpensive, is non-volatile, and allows code updates using an EPROM programmer system.

004 The second type of commonly utilized non-volatile memory device is the Electronically Erasable Programmable Read-Only Memory (EEPROM) class of memory devices. EEPROM devices are non-volatile memory devices that can be erased and programmed utilizing electrical signals. A typical EEPROM device includes several thousand-memory cells organized in an array. In general, a memory cell can includes a floating gate transistor and a select transistor.

005 This configuration is referred to as a two-transistor EEPROM cell. The select transistor in an EEPROM device is used to select memory cells that are to be erased or programmed. A selected memory cell refers to a memory cell that is either being programmed, erased, or read. On the other hand, unselected memory cells are the memory cells of the array that are not selected for programming, erasing, or reading. The floating gate transistors in the device are those transistors that store the digital data in each memory cell. The digital data can be stored as eight bit words called bytes. Each byte may be individually programmed and erased.

006 The third type of non-volatile memory that is generally used is Flash memory. Flash memory is another popular

form of non-volatile memory utilized in computers and other electronic devices. The terminology "flash" comes from the ability to simultaneously electrically erase an entire memory array or a large portion of the memory array in a flash. Flash memory is similar to EEPROM memory in function but must be erased in blocks, whereas EPROM can be erased one byte at a time. Flash EPROM (erasable programmable read-only memory) devices, in particular, have developed into a popular source of non-volatile, electrically erasable memory in a wide range of digital applications. Flash memory devices typically use a one-transistor memory cell, which permits high memory densities, high reliability, and low power consumption. These characteristics have made flash memory very popular for low power applications, such as battery-backed or embedded memory circuits.

007 Common uses of non-volatile memory include portable computers, personal digital assistant (PDA) devices, digital cameras, and cellular telephones. In these devices, both program code and system data, such as configuration parameters and other firmware, are often stored in flash memory because of the compact storage and relative ease of software upgradeability. The use of flash memory, for example, to store ungradable data has necessitated the development of mechanisms to protect the data from unintended erasure or reprogramming.

008 Memory arrays for use in non-volatile memory devices can be configured such that their memory cells are generally arranged in rows and columns. Typically, the gates of the transistors within the same row are connected to each other and to a common word line. Similarly, the drain electrodes of the transistors within the same column can be connected to each other and to a common bit line. In addition, the source electrodes of the transistors may be connected to each other via a common source line. To program a selected memory cell in a selected row and a selected column, a programming voltage can be applied to either or both the word line and the bit line which may be connected to the selected memory cell.

009 Memory arrays utilized to form EEPROM, EPROM, or Flash memory cells can use redundant memory elements (i.e., cells and accompanying word lines and bit lines organized as rows or columns) to compensate for production errors. Specifically, after the production of a complete memory array, a post-production test in the memory array can be generally performed. This post-production testing may indicate that a particular column, row or cell of the memory array is defective. A redundant memory element can then be substituted for the defective elements. This substitution typically occurs after the entire memory array has been manufactured. By allowing a defective memory element to be replaced by a redundant element after production, the memory array can still be used.

0010 Non-volatile memory can be utilized to store information necessary to repair defective rows and/or columns of memory arrays. The portion of the memory array that is utilized to store this repairing information or data can be referred to as the "information array." The repairing information is generally read-out to a volatile latch array after the associated computer system is powered-up. In order to save area or reduce associated circuit complexity, the information array can be placed together with the main array, such that both of these arrays share the same general "periphery circuit" and "bit lines." The repairing information, however, cannot be read-out correctly if the corresponding bit lines are defective. In other words, defective rows or columns cannot be repaired if the defective rows or columns itself are relied upon to read-out the information array. Thus, the repairing efficiency in such configurations is quite low.

0011 Based on the foregoing, the present inventor has come to the conclusion that a need exists for methods and systems, which would result in a dramatic increase in the repairing efficiency of columns in non-volatile memory arrays. The present inventor, in particular, has concluded that the utilization of an Error Correction Coding (ECC) scheme can assist in improving this repairing efficiency.

BRIEF SUMMARY OF THE INVENTION

0012 The following summary of the invention is provided to facilitate an understanding of some of the innovative features unique to the present invention, and is not intended to be a full description. A full appreciation of the various aspects of the invention can be gained by taking the entire specification, claims, drawings, and abstract as a whole.

0013 One aspect of the present invention provides methods and systems for repairing non-volatile memory.

0014 Another aspect of the present invention provides methods and systems for improving row and column repairing in non-volatile memory.

0015 Still another aspect of the present invention provides methods and systems for improving row and column repairing in non-volatile memory utilizing an error correcting coding (ECC) scheme.

0016 Yet another aspect of the present invention provides methods and systems for improving row and column repairing efficiency in non-volatile memory utilizing a redundancy scheme.

0017 The above and other aspects of the present invention are achieved as is now described. Methods and systems for improving repairing efficiency in non-volatile memory are

disclosed herein. Row and/or column repairing data may be read from an information array associated with the non-volatile memory. The repairing data is generally read to a volatile latch associated with the non-volatile memory. An error correction coding circuit (ECC) circuit can be enabled during reading of the repairing data to thereby identify and repair defective row or columns associated with the non-volatile memory, regardless of the corruption of the columns. The ECC circuit can thus be enabled during an access of a main array associated with the non-volatile memory to thereby correct correctable errors if a particular address corresponds to an address of a defective row or column. This particular address may comprise, for example, a Y-address corresponding to a defective column. When accessing an information row, the ECC function described herein can be unconditionally enabled to ensure that repairing information can be correctly read-out. When accessing the main array, such an ECC function is generally enabled if the Y-address is coincident with a failed Y-address.

0018 A read circuit is generally linked to the main array to thereby permit data to be read from the main array and transmitted to the ECC circuit. The ECC circuit is generally connected to the volatile latch to thereby permit data to be transferred from the ECC circuit to the volatile latch. The decoder circuit is generally linked to the ECC circuit, while the decoder circuit is generally linked to the information array, at least one spare row, and the main array, wherein the main array

can includes a normal array and one or more spare columns. The main array may also be linked to the information array such that the information array is considered part of the main array or a separate array, which shares the same circuit periphery with the main array. The volatile latch can be connected to the decoder circuit to thereby permit data contained within the volatile latch to be accessed by the decoder circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

0019 The accompanying figures, in which like reference numerals refer to identical or functionally-similar elements throughout the separate views and which are incorporated in and form part of the specification, further illustrate the present invention and, together with the detailed description of the invention, serve to explain the principles of the present invention.

0020 FIG. 1 illustrates a general microprocessor system in which a non-volatile memory device may be implemented in accordance with a preferred embodiment of present invention;

0021 FIG. 2 depicts a general microprocessor system in which a non-volatile memory device, specifically an EPROM, may be implemented in accordance with a preferred embodiment of present invention.

0022 FIG. 3 illustrates a general microprocessor system in which a non-volatile memory device, specifically an EEPROM, may be implemented in accordance with a preferred embodiment of present invention;

0023 FIG. 4 depicts a general microprocessor system in which a non-volatile memory device, specifically a flash memory device, may be implemented in accordance with a preferred embodiment of present invention;

0024 FIG. 5 illustrates a block diagram illustrative of a column repair scheme for non-volatile memory; and

0025 FIG. 6 depicts a block diagram illustrative of a column repair scheme for non-volatile memory utilizing an error correction coding (ECC) circuit, in accordance with a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

0026 The particular values and configurations discussed in these non-limiting examples can be varied and are cited merely to illustrate embodiments of the present invention and are not intended to limit the scope of the invention.

0027 FIGS. 1 to 4 illustrate a general microprocessor system in which a non-volatile memory device may be implemented in accordance with a preferred embodiment of present invention. In

FIGS. 1 to 4, analogous parts are indicated by identical reference numerals. Thus, a general non-volatile memory 14 is illustrated in FIG. 1, while other types of non-volatile memory devices are depicted in FIGS. 2 to 4. A computer system in which the various aspects of the present invention can be incorporated is thus illustrated generally in FIG. 1.

0028 A typical computer system architecture includes a microprocessor 10 connected to a system bus 20, along with random access memory (RAM), main system memory 22, and at least one or more input-output devices 24, such as a keyboard, monitor, modem, and the like. Another main-computer system component that can be connected to a typical computer system bus 22 is a large amount of long-term, non-volatile memory 14. Typically, such a memory is a disk drive with a capacity of tens of megabytes of data storage. This data can be retrieved into the main system memory 22 (i.e., volatile memory) for use in current processing, and can be easily supplemented, changed or altered.

0029 A memory controller 31 communicates with non-volatile memory 14 to form a bulk memory storage 26. Thus, bulk storage memory 26 can be constructed of a memory controller 12, connected to the computer system bus 20, and an array of non-volatile memory integrated circuit chips. Data and instructions can be communicated from memory controller 12 to such an array over a serial data line 18. Similarly, data and status signals may be communicated from non-volatile memory 14 to memory controller 12

over serial data lines 16. Other control and status circuits between memory controller 12 and non-volatile memory 14 are not shown in FIG. 1. Those skilled in the art can appreciate that the system depicted in FIGS. 1 to 4 is presented for illustrative purposes only.

0030 The bulk storage memory 26 of FIGS. 1 to 4 can be implemented on a single printed circuit card for moderate memory sizes. The system bus 20 may be terminated in connecting pins of such a printed circuit card for connection with the rest of the computer system through a connector (not shown in FIGS. 1 to 4). Also connected to the card and its components are various standard power supply voltages (not shown).

0031 There are a variety of non-volatile memory devices that may be utilized to implement non-volatile memory 14. Thus, as illustrated in FIG. 2, an EPROM 30 may be utilized. An EPROM (Erasable Programmable Read-Only Memory) is generally a type of non-volatile memory chip that can be programmed after it is manufactured. As depicted in FIG. 3, an EEPROM 34 may be relied upon as a non-volatile memory device. An Electrically Erasable and Programmable Read Only Memory ("EEPROM") is a non-volatile memory device that retains its memory even after power is shut down.

0032 Finally, as depicted in FIG. 4, a Flash memory 36 may be another type of non-volatile memory device that can be

utilized in accordance with the invention described and claimed herein. Flash memory is similar to EEPROM memory in function; however, it must be erased in blocks, whereas EEPROM can be erased one byte at a time. Because of its block-oriented nature, Flash memory is preferably utilized as a supplement to or replacement for hard disks in portable computers. Flash memory can either be constructed into the unit or available in the form of a PC card that can be plugged into a PCMCIA slot.

0033 Note that for a large amount of memory, a single array forming non-volatile memory 14 may not be sufficient. In such a case, additional EEPROM arrays can be connected to the serial data lines 18 and 16 of memory controller 12 (i.e., a controller chip). Such an arrangement may preferably be implemented on a single printed circuit card; however if space is not sufficient to accomplish this, then one or more EEPROM arrays may be implemented on a second printed circuit card that is physically mounted onto the first and connected to a common controller chip.

0034 FIG. 5 illustrates a block diagram 48 illustrative of a column repair scheme for non-volatile memory. Non-volatile memory can be utilized to store information or data regarding correction or repair of array rows and/or columns. A portion of non-volatile memory in which repair information is read out of memory is generally referred to as the "information array." Repairing information or data is thus read out of information

array 52 to a volatile latch array 60 after the associated computer system is powered-up (i.e., initiated).

0035 In order to save area or reduce the circuit complexity, information array 52 is generally placed with the main array 50. Main array 50 is composed of a spare row 54 and a section 56 comprising a "normal array" and a spare column. Thus, information array 52 and main array 50 share the same "periphery circuit" and "bit lines." The repairing information, however, cannot be read-out correctly if the corresponding bit lines are defective or corrupted. In other words, defective or corruptive columns may not be repaired if the defective or corrupted column is utilized to read-out information array 52.

0036 Note that in FIG. 5, main array 50 includes information array 52, spare row 54 and portion 56 (i.e. normal array and spare column). Those skilled in the art can appreciate, however, that in a varying embodiment of the present invention, information array 52 may be illustrated separate and apart from main array 50. The configuration depicted in FIG. 5 is thus presented for illustrative and educational purposes only and is not considered a limiting feature of the present invention.

0037 Main memory 50 is generally connected to a read circuit 58 for reading data from main memory 50. Data from read circuit 58 can in turn be transmitted to volatile latch array

60. A decoder circuit 62 (i.e., row/column decoder) is generally linked to information array 52, spare row 54, and portion 56 of main memory 50.

0038 FIG. 6 depicts a block diagram 49 illustrative of a column repair scheme for non-volatile memory utilizing an error correction coding (ECC) circuit, in accordance with a preferred embodiment of the present invention. Note that in FIGS. 5 and 6, analogous or similar parts are indicated by identical reference numerals. The configuration depicted in block diagram 49 thus depicts a redundancy scheme involving the use of Error correction coding (ECC) to improve the efficiency of column repairing. Error correction codes are generally utilized to correct certain classes of errors in memory storage devices, such as non-volatile memory devices, to greatly reduce the probability of an error affecting the memory output. ECC is generally an encoding method that permits the detection of errors that can occur during data storage and transmission.

0039 An error correction coding (ECC) circuit 70 is linked to volatile latch array 60, which in turn is connected to decoder circuit 62. ECC circuit 70 can be enabled through ECC enabling circuit 72, which is connected to ECC circuit 70. Read circuit 58 can access main memory 50 and transfer data to ECC circuit 70. To achieve improved column repair, information or data may be read from information array 52 to volatile latch array 60 after system power-up. During access of main array 50,

ECC circuit 70 is enabled to repair correctable errors if a Y-address corresponds to an address indicative of a corrupt or defective row and/or column. During the read-out of repairing information from information array 52, ECC circuit 70 is always enabled to repair any correctable errors of data. The correct repairing information can be read out of information array 52 even if some of the selected columns are defective or corrupted during access of information array 52.

0040 The configuration illustrated in FIG. 6 enables ECC circuit 70 to correct the correctable error when accessing repairing formation from information array 52. The repairing information can be read correctly even if defective or corrupted bits are present. This configuration thus improves the repairing efficiency when the information array 52 shares the same read/write circuit and bit lines with main array 50. If an ECC circuit, such as ECC circuit 70, is not available, defective bits in information array 52 will render the chip unrepairable.

0041 FIG. 6 thus depicts a configuration that may be utilized to improve column and/or row repairing efficiency in non-volatile memory devices, such as, for example, EPROM, EEPROM and Flash memory devices. Column and/or row repairing data may be read from information array 52, which is associated with the non-volatile memory and can form part of main array 50. This repairing data is generally read to a volatile latch (e.g., volatile latch array 60) associated with the non-volatile

memory. ECC circuit 70 can be enabled during reading of the repairing data to thereby identify and repair defective rows and/or columns associated with the non-volatile memory, regardless of the corruption of the columns. ECC circuit 70 can thus be enabled thus be enabled during an access of main array 50 (i.e., which is associated with the non-volatile memory) to thereby correct correctable errors if a particular address corresponds to an address of at least one defective row and/or column. This particular address may, for example, comprise a Y-address corresponding to a defective column or row.

0042 Read circuit 58 is generally linked to main array 50 to thereby permit data to be read from main array 50 and transmitted to ECC circuit 70. ECC circuit 70 is generally connected to volatile latch array 60 to thereby permit data to be transferred from ECC circuit 70 to volatile latch array 60. Decoder circuit 62 is generally linked to ECC circuit 70. Decoder circuit 62 is also generally linked to information array 52, spare row 54, and main array 50. Main array 50 can be configured to include a normal array and one or more spare columns.

0043 The number of spare columns depends on the coding of ECC circuit 70 and the maximum number of defective columns on a normal array that can be repaired. For example, in a scenario in which 512 columns are designated in a normal array, and a data bus comprises 16 bits, assuming that Hamming code (5,16) is

utilized and additionally assuming that the maximum number of defective columns that can be repaired is 4, then the number of spare columns required can be calculated as 20 based on the value 4x5. This holds true because 5 spare columns are generally required to repair 4 defective columns.

0044 Traditionally, one spare column is generally required to repair one defective column for one "specific IO" (i.e., there are 16IO if a data-bus is 16 bits). At least one spare column, however, must be placed per IO because the defective column could be located on any one IO. Thus, 16 spare columns are needed to repair one defective column. To improve the repairing efficiency, two IO with increasingly complicated designs could share one spare column. As a result, at least 8 spare columns may be required. Thus, in accordance with the method and system of the present invention, one or more spare columns (i.e., 5 in the aforementioned example) are required to repair one defective column in any IO. (Note that Hamming code (5,16) is well-known in the art and is described generally at pg. 64 of "Error Control Coding: Fundamentals and Applications," by Shu Lin & Daniel J. Costello, Jr.)

0045 Main array 50 may also be linked to information array 52, such that information array 52 is considered part of main array 50 or a separate array, which shares the same circuit periphery with main array 50. Volatile latch array 60 can be connected to decoder circuit 62 to thereby permit data contained

within volatile latch array 60 to be accessed by decoder circuit 62. Note that when accessing an information row, the ECC function is unconditionally enabled to make certain that repairing information will be correctly read-out. When accessing main array 50, the ECC function is generally enabled if the Y-address is coincident with a failed Y-address.

0046 The embodiments and examples set forth herein are presented to best explain the present invention and its practical application and to thereby enable those skilled in the art to make and utilize the invention. Those skilled in the art, however, will recognize that the foregoing description and examples have been presented for the purpose of illustration and example only. Other variations and modifications of the present invention will be apparent to those of skill in the art, and it is the intent of the appended claims that such variations and modifications be covered.

0047 The description as set forth is not intended to be exhaustive or to limit the scope of the invention. Many modifications and variations are possible in light of the above teaching without departing from scope of the following claims. It is contemplated that the use of the present invention can involve components having different characteristics. It is intended that the scope of the present invention be defined by the claims appended hereto, giving full cognizance to equivalents in all respects.